

Claims

1. A wide band modulation PLL, comprising:

a PLL part, including:

5 a voltage controlled oscillator;

a frequency divider that divides a frequency of an output
signal of the voltage controlled oscillator;

a phase comparator that outputs a signal based on a phase
difference between a reference signal and the output signal of the frequency
10 divider; and

a loop filter that outputs an output to the voltage controlled
oscillator so as to average the output of the phase comparator;

a first modulation input part that inputs a first modulation signal to the
voltage controlled oscillator based on inputted modulation data for modulating;

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a second modulation input part that inputs a second modulation signal
to a position different from the voltage controlled oscillator in the PLL part based
on the modulation data,

wherein the voltage controlled oscillator includes a first control terminal
20 to which the first modulation signal is inputted and a second control terminal to
which a signal based on the second modulation signal is inputted; and

wherein the first modulation input part has a modulation sensitivity
calculation unit that calculates a first modulation sensitivity in the first control
terminal and a modulation factor adjustment unit that adjusts a modulation
25 factor of the modulation data based on the calculated first modulation sensitivity

and outputs the first modulation signal.

2. The wide band modulation PLL as set forth in claim 1, wherein the modulation sensitivity calculation unit has a modulation sensitivity calculation part that measures a signal inputted to the second control terminal, that calculates a second modulation sensitivity in the second control terminal, that measures a value indicating a ratio between the second modulation sensitivity and the first modulation sensitivity, and that calculates the first modulation sensitivity based on the calculated second modulation sensitivity.

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3. The wide band modulation PLL as set forth in claim 1 or 2, wherein the first modulation input part has an A/D converter that makes digital conversion of a signal inputted to the second control terminal of the voltage controlled oscillator, the modulation sensitivity calculation unit, the modulation factor adjustment unit, and a D/A converter that makes analog conversion of an output of the modulation factor adjustment unit and that outputs the output to the first control terminal.

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4. The wide band modulation PLL as set forth in any one of claims 1 and 2, wherein the first modulation input part includes an A/D converter that makes digital conversion of a signal inputted to the second control terminal of the voltage controlled oscillator, the modulation sensitivity calculation unit, and the modulation factor adjustment unit;

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wherein the modulation factor adjustment unit outputs a digital signal to the first control terminal; and

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wherein the voltage controlled oscillator changes a frequency based on the digital signal inputted to the first control terminal.

5. The wide band modulation PLL as set forth in any one of claims 1 through 4, wherein the second modulation input part has a frequency dividing ratio generation unit that controls a frequency dividing ratio of the frequency divider based on carrier frequency data and the modulation data.

6. The wide band modulation PLL as set forth in any one of claims 1 through 4, wherein the second modulation input part has a direct digital synthesizer that generates a modulation signal based on carrier frequency data and the modulation data and that outputs the modulation signal to the phase comparator.

7. The wide band modulation PLL as set forth in any one of claims 1 through 6, wherein the first modulation input part calculates the first modulation sensitivity, adjusts a modulation factor and outputs the first modulation signal at the time of an activation of the wide band modulation PLL and every predetermined period is elapsed after the activation.

8. The wireless terminal apparatus incorporating the wide band modulation PLL according to any one of claims 1 through 7.

9. A modulation factor adjustment method of a wide band modulation PLL comprising a PLL part including a voltage controlled oscillator, a frequency

divider for dividing a frequency of an output signal of the voltage controlled oscillator, a phase comparator for outputting a signal according to a phase difference between a reference signal and an output signal of the frequency divider, and a loop filter for averaging an output of the phase comparator and

5 outputting the output to the voltage controlled oscillator, the method comprising:

inputting a first modulation signal to a first control terminal of the voltage controlled oscillator for modulating;

10 inputting a second modulation signal to a position different from the voltage controlled oscillator in the PLL part based on the PLL by inputting carrier frequency data;

calculating a first modulation sensitivity in the first control terminal of the voltage controlled oscillator, and

adjusting a modulation factor of the first modulation signal based on the calculated first modulation sensitivity.

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10. The modulation factor adjustment method of a wide band modulation PLL as set forth in claim 9, wherein the step of calculating the first modulation sensitivity comprises the steps of:

20 measuring an input voltage inputted to a second control terminal being different from the first control terminal in the voltage controlled oscillator based on the second modulation signal;

calculating a second modulation sensitivity in the second control terminal; and

25 measuring a value indicating a ratio between the second modulation sensitivity and the first modulation sensitivity, and calculating the first

modulation sensitivity based on the calculated second modulation sensitivity.